

# DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

# BTech in VLSI Design and Technology (Semiconductor)

#### **VISION**

- To become a pole of excellence in technical education, research and innovation by inculcating knowledge of science, engineering, technology and management for the growth of socially responsible individuals.
- To be recognized as a leader in ECE education and research, with state-of-the-art facilities and highly qualified faculty.
- To develop an innovative and industry-ready workforce that can provide technological solutions for the betterment of society.

#### **MISSION**

- To inculcate innovation, design, and entrepreneurship amongst the students through outcome-based learning
- To encourage and facilitate faculty, researchers, and students to work synergistically across the boundaries of various disciplines.
- To promote research and development, technical consultancy and symbiotic partnership between industry and the Institute with high regard for ethical principles and human values and to pursue knowledge as a process of lifelong learning.

# PROGRAMME EDUCATIONAL OBJECTIVES:

**PEO 1:** To prepare graduates with a strong foundation in mathematics, physics, semiconductor materials, and VLSI design principles to pursue successful careers in the semiconductor industry, research organizations, or higher studies.

**PEO 2:** To develop competent professionals with ethical responsibility, innovation mindset, and technical expertise capable of designing, fabricating, and managing advanced semiconductor and VLSI systems for sustainable technological growth.

# PROGRAM SPECIFIC OUTCOME (PSOs)

**PSO 1:** Graduates will be able to design, simulate, and implement analog, digital, and mixed-signal VLSI circuits and systems using industry-standard EDA and TCAD tools such as Cadence, Synopsys, and Mentor Graphics.

**PSO 2:** Graduates will possess the ability to analyze, model, and fabricate semiconductor devices and materials, contributing to advancements in microelectronics, nanoelectronics, and emerging quantum or neuromorphic technologies.



# **PROGRAMME OUTCOMES:**

PO1: Engineering Knowledge.

PO2: Problem Analysis.

PO3: Design/Development of Solutions.

PO4: Conduct Investigations of Complex Problems.

PO5: Engineering Tool Usage.

PO6: The Engineer and The World.

PO7: Ethics.

PO8: Individual and Collaborative Teamwork.

PO9: Communication.

PO10: Project Management and Finance.

PO11: Life-Long Learning.

# **Credit Definition**

Туре	Duration (in hours)	Credit
Lecture (L)	1	1
Tutorial (T)	1	1
Practical (P)	2	1

# **Total Credit Distribution for the Entire Programme**

C	Credits										C 1:4-/C
Semester	MC	ME	Projec	NM	NV	MDC	AE	SEC	VAC	INT	Credits/Semester
			t				$\mathbf{C}$				
1	15	0	0	0	0	0	3	2	0	0	18
2	15	0	0	0	0	0	0	4	2	0	20
3	22	0	0	0	0	0	0	1	0	0	22
4	17	0	0	0	0	0	3	1	0	0	21
5	20	0	0	0	0	0	3	1	0	0	24
6	13	5	0	0	0	0	0	2	0	0	20
7	0	0	4	0	0	9	3	0	0	2	18
8	0	0	18	0	0	0	0	0	0	0	18
<b>Total Credits</b>	102	5	22	0	0	9	12	11	2	2	161



# **Category Definition**

Definition of Category/Type	Abbreviation
Major Compulsory	MC
Major Elective	ME
Non-Major Specific Subject Course	NM
Non-major Vocational Education and Training	NV
Multidisciplinary Courses	MDC
Ability Enhancement Courses	AEC
Skill Enhancement Courses	SEC
Value Added Courses	VAC
Internship	INT



# FIRST YEAR

# **SEMESTER-I**

Sl	C T'41	C 1	T	C 1'4		Type	
No	Course Title	Code	Type	Credit	L	Т	P
1	Physics I	BS-01	MC	3	3	0	0
2	Mathematics-I	BS-02	MC	3	3	0	0
3	Basic Electrical Engineering	ES-01	MC	3	3	0	0
4	Engineering Graphics & Design	ES-02	MC	2	1	0	2
5	English for Technical Writing	HSM-01	AEC	3	2	0	2
6	CAD Tool-I	ES-093	SEC	2	0	0	4
7	Physics Lab	BS-091	MC	1	0	0	2
8	Basic Electrical Engineering Lab	ES-091	MC	1	0	0	2
9	IDEA Lab Workshop/Maker Space 1	AU-01	NV	0	0	0	3
10	3 WEEKS COMPULSORY INDUCTION PROGRAM (UHV-I)		VAC	0			
	Total Credits			18 Credits			

# **SEMESTER-II**

Sl	Course Title	Code	Tyres	Credit		Type	
No	Course Title	Code	Type	Credit	L	Т	P
1	Physics II	BS-03	MC	4	3	0	2
2	Mathematics-II	BS-04	MC	4	3	1	0
3	C Programming for Problem Solving	ES-04	MC	4	3	0	2
4	Basic Electronics	BS-05	MC	3	3	0	2
5	CAD Tool-II	ES-05	SEC	2	0	0	4
6	Linux and Scripting	SCC-10	SEC	2	1	0	2
7	Universal Human Values	HSM-02	VAC	2	2	0	0
8	Sports and Yoga or NSS/NCC	AU-02	NV	0	2	0	0
	Total Credits		20 Credits				



# **SECOND YEAR**

# **SEMESTER-III**

S1	Course Title	Codo	Т	Cua dia		Type	
No	Course Title	Code	Type	Credit	L	Т	P
1	Mathematics III	SCC-01	MC	3	3	0	0
2	Signal and System	SCC-02	MC	3	3	0	0
3	Data Structures	SCC-08	MC	3	3	0	2
4	Semiconductor Devices	PCC-01	MC	3	3	0	2
5	Analog Circuits	PCC-04	MC	3	3	0	2
6	Digital Logic Design	SCC-07	MC	3	3	0	2
7	Group Project 1/ Research Project 1/Specialization Elective/Microcredit Elective Course <i>with Industry</i>	PRC-01	PRJ*/S EC	1	0	0	2
8	Slot for BS Course	BS-06	MC	3	3	0	0
1 9	Slot for Mandatory Learning Course (Audit Course)	ML-01	AEC	0	0	0	0
10	Digital Electronics Lab		MC	1	0	0	2
	Total Credits				22 C1	redits	

# **SEMESTER-IV**

S1	Commo Title	Codo	Т	Con dia		Type	
No	Course Title	Code	Type	Credit	L	Т	P
	Computer and Processor Architecture	SCC-04	MC	3	3	0	0
2	Quantum Devices and Circuits	SCC-05	MC	2	2	0	0
3	Communication Engineering	SCC-03	MC	3	2	0	2
1 4	Photonics and Optoelectronics Devices	PCC-02	MC	3	2	0	2
· •	Micro-fabrication and Semiconductor materials	PCC-03	MC	3	3	0	0
6	Electromagnetism for VLSI	SCC-06	MC	3	2	0	2
7	Group Project 2/ Research Project 2/Specialization Elective/Microcredit Elective Course	PRC-02	PRJ*/S EC	1	0	0	2
8	Slot for HM Course	HSM-03	AEC	3	3	0	0
	Total Credits				21 C1	redits	



# THIRD YEAR

# SEMESTER-V

S1	Course Title	Cada	Т	Cua dia		Type	
No	Course Title	Code	Type	Credit	L	Т	P
	SOC Design: Design & Verification	PCC-05	MC	3	2	0	2
	Compound Semiconductor Devices	PCC-06	MC	3	2	0	2
3	CMOS Integrated Circuits	PCC-07	MC	5	3	0	4
4	Electronic System Design	PCC-08	MC	5	3	0	4
5	MEMS and NEMS	PCC-09	MC	2	2	0	0
6	Memory Design	PCC-10	MC	2	2	0	0
7	Group Project 3/ Research Project 3 on Semiconductor Modelling and Simulations	PRC-03	PRJ*/S EC	1	0	0	2
8	Slot for HM Course	HSM-04	AEC	3	3	0	0
	Slot for Mandatory Learning Course (Audit Course)	ML-03	AEC	0	0	0	0
	Total Credits	24 Credits					

# **SEMESTER-VI**

S1	Commo Title	Codo	Т	C 1:4		Type	
No	Course Title	Code	Type	Credit	L	T	P
1	Mixed mode VLSI Circuit	PCC-11	MC	4	3	0	2
2	IC Packaging	PCC-12	MC	3	2	0	2
4	Semiconductor Materials Synthesis and Characterization	PCC-13	MC	3	3	0	0
1 /1	Semiconductor Manufacturing: Materials and Process	PCC-14	MC	3	3	0	0
5	Group Project 4/ Research Project 4/Specialization Elective/Microcredit Elective Course		PRJ*/S EC	2	0	0	4
6	Program Elective-01	PE-01	ME	2	2	0	0
7	Program Elective-02	PE-02	ME	3	3	0	0
	Total Credits	20 Credits					



# **FOURTH YEAR**

# **SEMESTER-VII**

Sl	Covera Title	Cada	Т	C 1:4		Type	
No	Course Title	Code	Type	Credit	L	Т	P
1	Open Elective-01 (Online)	OE-01	OE	3	3	0	0
2	Open Elective-02 (Online)	OE-02	OE	3	3	0	0
3	Open Elective-03 (Online)	OE-03	OE	3	3	0	0
4	Slot for HSM Course (Online)	HSM-5	AEC	3	3	0	0
5	Internship/Foundry visits	XC-28	INT	2	0	0	10
6	Final Year Project Phase -1	XC-29	PRJ	4	0	0	4
	Total Credits	18 Credits					

# **SEMESTER-VIII**

Sl	Course Title	Code	Tuna	Credit	Type				
No	Course Title	Code	Type	Credit	L	Т	P		
1	Final Year Project Phase 2	XC-P3	PRJ	18	0	0	36		
	Total Credits				18 C	redits			



# COURSE CO-PO-PSO MAPPING SEMESTER-I

## **COURSE 2 (Mathematics-I)**

#### **COURSE OUTCOMES:**

**CO1:** Illustrate the concepts of determinants, matrices, and vector algebra to solve systems of linear equations.

CO2: Implement vector space principles and linear algebraic tools in various physical and computational problems.

**CO3:** Examine first- and second-order differential equations to solve them using appropriate analytical methods.

**CO4:** Detect singularities in the process of evaluation of complex integral in mathematical modeling and engineering applications.

**CO5:** Construct transformations of complex functions using conformal mapping and Mobius transformation for advanced problem.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	PROGRAMME OUTCOMES											PROGRAMME SPECIFIC OUTCOMES		
ES	PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO10 PO11										PSO1	PSO2	PSO3		
CO1	3	3	3	2	2		2	1				1	2	1	
CO2	3	3	3	3	2			1			1	2	3	2	
CO3	2	3	2	1	3		1	1	2			1	2	2	
CO4	3	2 3 2 1 2 1 1											3	1	
CO5	3	3	3	2	2			1	2	1	1	1	3	2	

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 3 (Basic Electrical Engineering)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental laws, theorems, and behavior of basic DC and AC circuits.

**CO2:** Analyze single-phase and three-phase AC circuits and apply network theorems to solve electrical problems.

**CO3:** Describe the construction, working, and performance of electrical machines and transformers.

**CO4:** Apply basic power converter principles (DC–DC and DC–AC) for electrical energy conversion and control.

**CO5:** Design and analyze passive and active filter circuits using operational amplifiers for signal conditioning.



## MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	COME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PSO1	PSO2								
CO1	3	3	2	2	0	2	2						
CO2	3	3	3	3	3	1	1	1	0	1	1	2	2
CO3	3	3	3	2	2	1	2	1	1	1	1	3	2
CO4	3	3	3	3	3	1	2	1	1	1	1	3	3
CO5	3	3	3	3	3	1	2	1	2	2	2	3	3

1. LOW 2. M

2. MODERATE

3. SUBSTANTIAL

# **COURSE 4 (Engineering Graphics & Design)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the ISO standards for technical drawing, including line types, paper sizes, layout, and various types of projections.

**CO2:** Apply various dimensioning techniques (chain, parallel, combined, coordinate) to represent the size and location of features on different mechanical parts.

**CO3:** Analyze and indicate different types of tolerances (linear, angular, geometrical, bilateral, unilateral) and fits on part drawings to define manufacturing requirements.

**CO4:** Draw standard engineering curves (conic sections) and represent different trade-related symbols for fasteners, welding, and electrical elements.

**CO5:** Prepare professional part drawings and freehand sketches of simple tools and objects following all standard conventions, sections, and assembly indications.

# **MAPPING OF COS WITH POS AND PSOS**

OUTCOM	PRO	GRA	MME	COUT	COM	IES						SPEC	RAMME IFIC COMES
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	-	-	-	1	-	-	-	1	-	1	1	1
CO2	3	2	2	-	1	-	-	-	1	-	1	2	1
CO3	3	3	3	1	-	1	-	1	2	1	1	2	1
CO4	3	-	2	-	-	-	-	-	1	-	1	1	1
CO5	3	2	3	1	2	1	-	2	3	2	2	3	2

1. LOW

2. MODERATE



# **COURSE 5 (English for Technical Writing)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamentals of communicative English and demonstrate an understanding of general communication skills.

CO2: Identify nuances in intonation and apply correct pronunciation techniques to enhance spoken communication.

CO3: Use essential grammatical structures and develop foundational language skills for accurate communication.

**CO4:** Build and employ an extensive English vocabulary to improve language proficiency and express ideas effectively.

**CO5:** Integrate grammar, pronunciation, and vocabulary skills to communicate confidently and appropriately across diverse contexts

## MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	C OUT	COM	1ES						SPE	GRAN CIFIC COM	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	2	3		2	1				1	2	1
CO2	3	3	3	3	2		2	1			1	2	3	2
CO3	3	2	2	2	3		1	2	2	2		2	1	2
CO4	2	2	3	1	1		2	1	2		2	2	3	3
CO5	3	3	3	2	2			1	1	1	1	1	3	2

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 6 (CAD Tool-I)**

#### **COURSE OUTCOMES:**

**CO1:** Demonstrate the setup and operation of Cadence and Synopsys TCAD tools for semiconductor device simulation.

**CO2:** Simulate and analyze DC and AC responses of basic electronic circuits such as resistive and CMOS inverters using Cadence.

CO3: Examine the transient and frequency response characteristics of RC low-pass filters through simulation.

**CO4:** Investigate and interpret the V–I characteristics of semiconductor devices such as the pn diode using both Cadence and Synopsys TCAD platforms.

**CO5:** Examine DC and AC analysis of pn junction devices using TCAD simulation tools and correlate results with theoretical predictions.



OUTCOM	PRO	GRA	MME	OUT	COM	ES					PROG SPECI OUTC	
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2					
CO1	3	2	2	2	3		1	2	2	1	3	2
CO2	3	3	3	2	3			1	2	1	3	2
CO3	2	3	2	2	3			1	2	1	3	2
CO4	2	3	2	3	3		1	1	2	1	2	3
CO5	2	3	2	3	3		1	1	2	1	2	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 8 (Basic Electrical Engineering Lab)**

# **COURSE OUTCOMES:**

**CO1:** Apply circuit-theory theorems to solve practical networks.

**CO2:** Analyze power transfer and optimize load conditions.

CO3: Measure and characterize resonant circuits and frequency response.

**CO4:** Determine two-port parameters and design/analyze filters.

**CO5:** Use circuit-simulation tools to model, verify and report results.

COURSE OUTCOMES	PRO	GRA	MME	OUT	COM	IES						E SPE	RAMM CIFIC OMES
	<b>PO</b> 1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	3	2	2	3				1	1	1	2	1
CO2	3	3	3	2	2				1	1	1	2	2
CO3	2	3	2	3	3				1	1	1	3	2
CO4	2	3	3	2	3			1	1	2	1	3	3
CO5	2	2	2	3	3			1	2	2	2	3	2

1. LOW

2. MODERATE



#### **SEMESTER-II**

# **COURSE 2 (Mathematics-II)**

#### **COURSE OUTCOMES:**

**CO1:** Explain fundamental concepts of matrices, determinants, eigenvalues, eigenvectors, and first-order ordinary differential equations.

**CO2:** Apply matrix methods, Laplace transforms, and Fourier analysis to solve linear systems and differential equations.

**CO3:** Analyze the behavior of differential equations using analytical techniques.

**CO4:** Examine solutions of ordinary differential equations and systems of equations.

**CO5:** Formulate mathematical models to solve real-world physical and engineering problems.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM ES					PROG	GRAN	IME O	UTCO	MES			ME SPE	GRAM CIFIC COME
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	_	_	_	_	<u> </u>	_	_	_	_	_	_	_
CO2	3	3	_		2	_					_	3	_
CO3	2	3	_	3	3	_	_	_	_	_		3	2
CO4	2	3	-	3	2	2	_	_		_	_	2	3
CO5	3	2	3		3						3	3	3

1. LOW 2. MODERATE 3. SUI

3. SUBSTANTIAL

# **COURSE 4 (Basic Electronics)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental principles of semiconductor physics and the operational characteristics of diodes, BJTs, and FETs.

**CO2:** Solve for the DC operating points and AC parameters of various BJT and FET biasing and amplifier circuits.

**CO3:** Analyze the performance, frequency response, and stability of transistor-based amplifier and feedback circuits.



**CO4:** Analyze the operation and output waveforms of diode-based application circuits,

including rectifiers, clippers, and clampers.

CO5: Design functional analog circuits, such as filters, oscillators, and mathematical operators, using operational amplifiers.

OUTCOM	PRO	GRA	MME	OUT	COM	ES						SPE(	GRAMME CIFIC COMES
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO 1	PSO2
CO1	3	1									1	1	
CO2	3	3	1	1							1	2	
CO3	3	3	2	2							1	2	
CO4	3	2	1	1								1	
CO5	3	3	3	2	2						1	2	

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 5 (CAD Tool-II)**

# **COURSE OUTCOMES:**

**CO1:** Explain the purpose and operational workflow of EDA tools for circuit simulation (Cadence) and device simulation (TCAD).

**CO2:** Use the Cadence simulation environment to build schematics and test the functionality of analog and digital circuits.

**CO3:** Analyze simulation data to extract the DC/AC performance characteristics of MOSFETs and operational parameters of amplifiers.

**CO4:** Compare the simulated behavior of circuits, such as amplifiers and logic gates, against their expected theoretical performance.

**CO5:** Construct device structures and circuit schematics within software tools to generate data for performance analysis.

OUTCOM	PRO	PROGRAMME OUTCOMES PO1 PO2 PO3 PO4 PO5 PO6 PO7 PO8 PO9 PO1									E SP	GRAMM ECIFIC COMES	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO 1	PSO2
CO1	3				2						1	2	
CO2	2		2		3			2	2			3	





CO3	2	3		2	3		2	2		3	
CO4	3	3		3	3		2	2		3	1
CO5	2		3	2	3		2	2	1	3	2

1. LOW

2. MODERATE



## **SEMESTER-III**

# **COURSE 1 (Mathematics III)**

#### **COURSE OUTCOMES:**

**C01:** Recall fundamental concepts of probability theory, set algebra, and key probability distributions along with their properties.

**C02:** Apply statistical methods such as maximum likelihood estimation and confidence intervals to estimate parameters for real-world problems.

C03: Analyze joint probability distributions, functions of random variables, and sampling distributions to solve complex statistical problems.

**C04:** Evaluate the appropriateness of different probability models and hypothesis tests for given data sets and research questions.

**C05:** Construct probabilistic models for engineering applications by integrating concepts of random variables, transformations, and limit theorems.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	ROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO5	PO1 0	PO1 1	PSO1	PSO2				
C01	3	1	-	-	1	1	1						
C02	3	2	2	1	2	1	-	-	-	-	2	1	2
C03	3	3	2	2	2	1	-	ı	-	-	2	2	2
C04	3	3	2	3	2	2	1	-	-	-	2	2	2
C05	3	3	3	2	2	2	-	2	2	2	2	2	2

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 2 (Signal and System)**

## **COURSE OUTCOMES:**

**CO1:** Classify different types of signals and systems based on their properties and characteristics.

CO2: Apply mathematical transforms (Laplace, Fourier, Z-transform) to analyze continuous



and discrete-time signals.

**CO3:** Analyze the behavior of linear time-invariant (LTI) systems in both time and frequency domains.

**CO4:** Evaluate system properties such as stability, causality, and linearity using transform domain techniques.

**CO5:** Design appropriate signal processing techniques for solving engineering problems using transform methods.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	ROG	RAM	ME (	OUTC	COME	LS			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	1	-	-	-	-	-	-	1	-	1	2	1
CO2	3	2	2	-	2	-	-	-	-	-	2	2	2
CO3	3	3	2	2	2	-	-	-	-	-	2	2	2
CO4	3	3	2	3	2	-	-	-	-	-	2	2	2
CO5	3	3	3	2	2	1	-	2	2	1	2	3	2

1. LOW

2. MODERATE

3. SUBSTANTIAL

## **COURSE 3 (Data Structures)**

#### **COURSE OUTCOMES:**

**C01:** Describe the properties, operations, and implementation techniques of fundamental linear data structures such as arrays, linked lists, stacks, and queues.

C02: Implement non-linear data structures including trees and graphs using object-oriented programming principles.

**C03:** Apply appropriate sorting and searching algorithms to solve computational problems and analyze their time complexity.

C04: Differentiate between various data structure types and algorithms to select the most efficient solution for a given problem.

**C05:** Design and develop a software application by integrating multiple data structures and algorithms to address a complex computational task.



## MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	1	1
C02	3	2	2	-	3	-	-	-	-	-	2	2	2
C03	3	3	2	2	3	-	-	-	-	-	2	2	2
C04	3	3	2	2	2	1	-	-	-	-	2	2	2
C05	3	3	3	2	3	1	-	2	2	2	3	2	2

1. LOW 2. MODERATE

3. SUBSTANTIAL

# **COURSE 4 (Semiconductor Devices)**

#### **COURSE OUTCOMES:**

**C01:** Explain the fundamental principles of semiconductor physics, including band diagrams, carrier transport, and the operation of a PN junction under bias.

C02: Analyze the electrical characteristics of diodes and transistors (JFET, MOSFET, BJT) to determine their regions of operation.

C03: Design and evaluate basic electronic circuits such as rectifiers, clippers, and digital switches using diodes and MOSFETs.

**C04:** Compare the operation, characteristics, and performance metrics of different transistor types, including JFETs, MOSFETs, and BJTs.

**C05:** Propose suitable semiconductor devices, including emerging technologies like FinFETs, for specific applications by evaluating factors such as scaling and short-channel effects.

# MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	2	3
C02	3	3	1	2	-	-	-	-	-	-	2	2	3
C03	3	2	3	1	2	1	-	-	-	-	2	3	2





C04	3	3	2	2	-	-	-	-	-	-	2	2	3
C05	3	3	3	3	-	2	1	1	2	1	3	3	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 5 (Analog Circuits)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the operation of semiconductor devices and their role in basic electronic circuits.

**CO2:** Apply biasing techniques and small-signal models to analyze BJT and FET amplifier circuits.

**CO3:** Analyze frequency response, feedback effects, and multistage amplifier performance.

**CO4:** Evaluate operational amplifier-based linear and non-linear applications with respect to design requirements.

**CO5:** Design regulated power supplies and active filter circuits to meet specified electronic applications.

# **MAPPING OF COS WITH POS AND PSOS**

COURSE OUTCOM			P	PROG	RAM	IME (	OUTC	COME	ES			PROGRA SPECI OUTCO	IFIC
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
C01	3	1	-	-	-	-	-	-	1	-	1	2	2
C02	3	3	2	1	2	-	-	-	-	-	2	3	2
C03	3	3	2	2	2	-	-	-	-	-	2	3	2
C04	3	3	2	3	2	1	-	-	-	-	2	3	2
C05	3	3	3	2	3	2	_	2	2	2	2	3	2

1. LOW

2. MODERATE



# **COURSE 6 (Digital Logic Design)**

#### **COURSE OUTCOMES:**

**C01:** Apply Boolean algebra to simplify and analyze the behavior of combinational logic circuits.

C02: Design sequential logic circuits, including state machines, using flip-flops and logic gates.

C03: Implement digital systems such as arithmetic circuits, counters, and shift registers using hardware description languages (HDLs) and FPGAs.

**C04:** Differentiate between the functions and applications of various memory devices and microprocessor fundamentals.

**C05:** Construct and troubleshoot a complete digital system by integrating combinational and sequential components for a specified application.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	ROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	IFIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	2	1	-	-	-	-	-	-	-	1	2	1
C02	3	3	3	1	1	-	-	-	-	-	2	3	1
C03	3	2	3	-	3	-	-	1	-	-	2	3	2
C04	3	2	2	-	-	-	-	-	-	-	2	2	2
C05	3	3	3	2	3	1	-	2	2	2	3	3	2

1. LOW

2. MODERATE



## **SEMESTER-IV**

# **COURSE 1 (Computer and Processor Architecture)**

#### **COURSE OUTCOMES:**

C01: Explain the fundamental principles of instruction set architecture and processor design.
C02: Analyze the performance of a processor by applying the concepts of pipelining and cache memory organization.
C03: Evaluate the efficiency of a computer architecture by examining its memory hierarchy and input/output system organization.
C04: Design the core components of a modern processor, including arithmetic and logic units, based on system requirements.
C05: Formulate a strategy for an energy-efficient system-on-chip (SoC) design by integrating principles of parallel processing and emerging technologies.

# MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 0	PO1 1	PSO1	PSO2					
C01	3	1	-	-	-	-	-	-	1	-	1	2	1
C02	3	3	2	2	2	-	-	-	-	-	2	2	2
C03	3	3	2	3	2	1	-	-	-	-	2	2	2
C04	3	3	3	2	2	-	-	-	-	-	2	3	2
C05	3	3	3	3	2	2	1	2	2	2	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 2 (Quantum Devices and Circuits)**

## **COURSE OUTCOMES:**

**C01:** Describe the fundamental concepts of qubits, quantum superposition, and entanglement using Dirac notation.



C02: Differentiate between various physical implementations of qubits, such as superconducting circuits and trapped ions, by comparing their properties.

C03: Construct quantum circuits by applying single and multi-qubit gates to implement basic quantum algorithms.

**C04:** Analyze the impact of decoherence and noise on quantum systems and evaluate the role of quantum error correction codes

**C05:** Design a conceptual setup for a quantum application, such as a key distribution system or a simple processor, by integrating principles of device fabrication, control, and measurement.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	COME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	2	2
C02	3	3	2	2	-	-	-	-	-	-	2	2	3
C03	3	2	3	1	2	-	-	-	-	-	2	3	2
C04	3	3	2	3	2	-	-	-	-	-	2	2	3
C05	3	3	3	3	2	2	1	2	2	2	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 3 (Communication Engineering)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamentals of analog communication systems

**CO2:** Demonstrate the generation and detection methods for modulation system, along with the principle of superheterodyne receivers.

CO3: Define the concepts of frequency and phase modulation, their generation and detection methods, and check their performance using mathematical tools.

**CO4:** Examine the concepts of multiplexing, noise sources, and signal-to-noise ratio (SNR) in analog communication systems.

**CO5:** Solve the probability and random variable theory to model noise in communication systems and assess system performance under different noise environments.



## MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	COME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 0	PO1 1	PSO1	PSO2					
C01	3	1	-	-	1	1	1						
C02	3	2	2	-	2	-	-	-	-	-	2	2	1
C03	3	2	2	1	2	-	-	-	-	-	2	2	1
C04	3	3	2	2	2	1	-	-	-	-	2	2	1
C05	3	3	2	3	2	1	-	-	-	-	2	2	2

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 4 (Photonics and Optoelectronics Devices)**

#### **COURSE OUTCOMES:**

C01: Explain the fundamental principles of optical interband transitions, including spontaneous and stimulated emission semiconductors. in C02: Design photodetector and solar cell devices by applying the principles of optical limits photovoltaic absorption and fundamental the of C03: Analyze the operational principles of semiconductor optical amplifiers, lasers, and LEDs evaluate their performance characteristics. C04: Differentiate between the operating mechanisms and applications of display technologies, **OLEDs** and including LCDs. C05: Formulate the design for an integrated optoelectronic system by combining components such as waveguides, lasers, and displays for a specific application.

# MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	ROG	RAM	ME (	OUTC	COME	ES			PROGRA SPECI OUTCO	IFIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	2	3
C02	3	3	3	2	2	2	-	-	-	-	2	3	3
C03	3	3	2	3	2	-	-	-	-	-	2	3	3
C04	3	2	2	2	-	1	-	-	-	-	2	2	2
C05	3	3	3	3	2	2	1	2	2	2	3	3	3



# 1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 5 (Micro-fabrication and Semiconductor materials)**

#### **COURSE OUTCOMES:**

CO1: Explain the key processes involved in semiconductor manufacturing and fabrication.

CO2: Compare various lithography techniques used for pattern transfer in IC fabrication.

CO3: Analyze the mechanisms of oxidation, diffusion, and ion implantation for doping semiconductors.

**CO4:** Evaluate different thin film deposition techniques and their applications in VLSI technology.

**CO5:** Differentiate between MOS and Bipolar fabrication processes based on their steps and device characteristics.

#### MAPPING OF COS WITH POS AND PSOS

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	2	3
C02	3	2	2	2	-	-	-	-	-	-	2	2	3
C03	3	2	2	2	-	-	-	-	-	-	2	2	3
C04	3	2	2	2	-	-	-	-	-	-	2	2	3
C05	3	3	2	2	-	-	-	-	-	-	2	2	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 6 (Electromagnetism for VLSI)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental laws of electromagnetics, vector calculus, and plane wave propagation in different media.

**CO2:** Apply transmission line concepts and Smith chart techniques to solve impedance matching and power transfer problems.



**CO3:** Analyze wave propagation characteristics in guided structures such as parallel plane and rectangular waveguides.

**CO4:** Evaluate electromagnetic interference and compatibility issues in practical electronic and communication systems.

CO5: Design basic antenna structures and predict their radiation parameters for efficient communication.

# **MAPPING OF COS WITH POS AND PSOS**

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGRA SPECI OUTCO	FIC
ES	PO1	PO2	PO3	PO4	PO1 1	PSO1	PSO2						
C01	3	1	-	-	-	-	-	-	1	-	1	2	2
C02	3	3	2	1	2	-	-	-	-	-	2	2	2
C03	3	3	2	2	2	-	-	-	-	-	2	2	2
C04	3	3	2	3	2	2	2	-	-	-	2	3	2
C05	3	3	3	2	2	1	-	-	-	-	2	3	2

1. LOW

2. MODERATE



## **SEMESTER-V**

# **COURSE 1 (SOC Design: Design & Verification)**

#### **COURSE OUTCOMES:**

**CO1:** Understand the fundamental concepts of SoC chip design.

**CO2:** Implement basic techniques for integrating IPs into SoC.

**CO3:** Apply simulation toolboxes for real-time applications.

**CO4:** Examine the hardware validation related to FPGAs.

**CO5:** Demonstrate rapid prototyping with FPGAs.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	COUT	COM	IES						PROGE SPECE OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	3	1	3	-	-	-	3	1	1	3	3
CO2	3	2	2	2	3	-	-	-	-	-	2	3	2
CO3	3	2	2	2	3	-	-	-	2	-	2	2	3
CO4	3	3	3	2	3	-	-	-	2	-	2	3	2
CO5	3	3	3	3	3	-	-	-	2	1	2	2	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 2 (Compound Semiconductor Devices)**

#### **COURSE OUTCOMES:**

**CO1:** Understand the fundamental concepts of semiconductor theory.

CO2: Utilize the characteristics of different advanced semiconductor devices with its applications.

CO3: Distinguish between different compound semiconductor devices and their real-time usability.

**CO4:** Analyze transistor amplifiers with small scale signal model.

**CO5:** Examine the use of FET amplifiers using small signal model.



# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	IES						PROGRA SPECIFI OUTCO	(C
ES	PO1	PO2	PO3	PO4	PO5	PO10	PO11	PSO1	PSO2				
CO1	3	3	2	1	3	-	-	-	3	1	1	3	3
CO2	3	3	3	2	3	-	-	-	-	-	2	2	3
CO3	3	2	2	2	3	-	-	-	2	-	2	3	2
CO4	3	3	3	2	3	_	_	-	2	_	2	3	2
CO5	3	3	3	3	3	_	-	-	2	1	2	2	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 3 (CMOS Integrated Circuits)**

#### **COURSE OUTCOMES:**

**CO1:** Understand the basics of CMOS logic circuits and various steps involved in the design of Integrated circuits.

CO2: Explain delay models, logical effort of path and various types of power dissipation.

CO3: Execute the concept of Dynamic, Domino CMOS logic.

**CO4:** Compare power logic circuits and different semiconductor memories used in present day technology.

CO5: Examine faults in digital circuits, Fault Models and various Testing Methodologies.

#### **MAPPING OF COS WITH POS AND PSOS**

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	AS.			PROGR SPEC OUTC	CIFIC
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	2	3	2	1	1	1	1	3	3	3
CO2	3	3	2	3	3	3	1	1	1	1	3	3	3
CO3	2	2	2	1	1	2	2	3	3	3	2	3	2
CO4	3	3	3	3	2	2	2	2	1	1	3	2	3
CO5	3	3	3	2	3	3	2	1	1	1	3	3	2

1. LOW

2. MODERATE



# **COURSE 4 (Electronic System Design)**

#### **COURSE OUTCOMES:**

**CO1:** Understand the fundamental concepts of digital system design principles.

CO2: Implement basic digital components and their practical utility in designing VHDL.

**CO3:** Apply digital Systems on the FPGAs.

**CO4:** Examine the System-Level design and integration.

CO5: Demonstrate VHDL for the deployment of combinational and sequential circuits.

# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROG E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	2	2	1	1	1	0	1	0	2	2
CO2	3	3	3	3	3	1	1	1	0	1	1	3	3
CO3	3	3	3	3	3	1	2	1	1	2	2	3	3
CO4	3	3	3	3	3	1	2	1	2	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 5 (MEMS and NEMS)**

#### **COURSE OUTCOMES:**

**CO1:** Define the basic properties of semiconductors and solid mechanics to fabricate MEMS and NEMS devices.

**CO2:** Utilize the rudiments of Micro fabrication techniques.

**CO3:** Distinguish various types of sensors and actuators.

**CO4:** Verify the concept relating to different materials used for MEMS and NEMS.

**CO5:** Implement various applications of MEMS and NEMS.

# **MAPPING OF COS WITH POS AND PSOS**

COURSE OUTCOM			P	PROG	RAM	ME (	OUTC	OME	ES			PROGR SPEC OUTC	CIFIC
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	2	2	1	3	-	-	1	3	1	1	3	3
CO2	3	3	2	2	3	-	-	1	-	-	2	3	2





CO3	3	3	3	2	3	2	1	-	2	-	2	2	2
CO4	3	3	3	2	3	-	1	1	2	-	2	2	3
CO5	3	3	3	3	3	2	1	-	2	1	2	3	2

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 6 (Memory Design)**

# **COURSE OUTCOMES:**

**CO1:** Understand the fundamental principles and working mechanisms of various memory technologies, including SRAM, DRAM, and non-volatile memories.

**CO2:** Compare advanced memory technologies such as FRAM, MRAM, and experimental memory devices for their advantages and limitations.

CO3: Analyze different memory architectures and their applications in modern computing systems.

**CO4:** Apply knowledge of memory technologies to design and optimize memory systems for specific applications.

**CO5:** Implement various type of memory cells used in the real-world applications.

# **MAPPING OF COS WITH POS AND PSOS**

OUTCOM	PRO	GRA	MME	OUT	COM	IES						SPEC	RAMME IFIC COMES
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	3	2	2	1	1	1	1	3	2	2
CO2	3	3	2	2	3	3	1	1	1	1	3	3	3
CO3	2	2	3	1	1	2	2	3	3	3	2	2	2
CO4	3	3	3	3	2	3	2	2	1	1	3	1	3
CO5	3	3	2	2	3	3	2	1	1	1	3	2	3

1. LOW

2. MODERATE



## **SEMESTER-VI**

# **COURSE 1 (Mixed mode VLSI Circuit)**

#### **COURSE OUTCOMES:**

**CO1:** Understand and analyze the principles of analog and discrete-time signal processing, including sampling theory, Z-transform, and filter design.

**CO2:** Design and evaluate switched-capacitor filter architectures considering non-idealities and mixed-signal applications.

**CO3:** Compare and implement data converter architectures such as SAR, flash, pipeline, and hybrid ADCs/DACs for target performance metrics.

**CO4:** Analyze and design mixed-signal circuits for data transmission and frequency synthesis, including voltage/current-mode signaling, PLLs, and DLLs.

**CO5:** Develop and simulate a complete mixed-signal subsystem integrating analog and digital components using industry-standard tools.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROG E SPE OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	3	2	2	2	1	1	1	0	1	0	2	3
CO2	3	3	3	3	3	1	1	1	0	1	0	3	3
CO3	3	3	3	3	3	1	2	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 2 (IC Packaging)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the evolution, classification, and materials used in IC packaging, along with interconnection and assembly techniques.

CO2: Analyze thermal, signal, and power integrity challenges in IC packaging and propose



suitable design strategies.

**CO3:** Evaluate reliability factors, mechanical stresses, and material interactions affecting package performance.

**CO4:** Design optimized IC packaging solutions considering electrical, thermal, and mechanical trade-offs using modern CAD tools.

**CO5:** Investigate and present project-based studies on emerging IC packaging materials, technologies, and applications.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	3
CO2	3	3	3	3	3	1	2	1	0	1	0	3	3
CO3	3	3	3	3	3	1	3	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	2	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

## **COURSE 3 (Semiconductor Materials Synthesis and Characterization)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental concepts of semiconductor materials, including crystal structures, band theory, and emerging materials such as perovskites and 2D semiconductors.

**CO2:** Describe and compare semiconductor synthesis techniques such as bulk crystal growth, thin film deposition, and epitaxial methods.

**CO3:** Analyze the effects of structural and chemical defects on electrical and optical properties of semiconductors and suggest mitigation strategies.

**CO4:** Apply appropriate characterization techniques to evaluate structural, optical, and electrical properties of semiconductor materials.

**CO5:** Assess the suitability of synthesized and characterized materials for advanced electronic and optoelectronic device applications.



## MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	3
CO2	3	3	2	2	3	1	2	1	0	1	0	2	3
CO3	3	3	3	3	3	1	2	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	1	1	3	3
CO5	3	3	3	3	3	2	3	1	2	3	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 4 (Semiconductor Manufacturing: Materials and Process)**

#### **COURSE OUTCOMES:**

**CO1:** Explain the types, functions, and evolution of semiconductor packaging materials, including substrates, die attach, and encapsulants.

**CO2:** Describe and analyze the properties, selection criteria, and fabrication processes of packaging and interconnect materials.

**CO3:** Evaluate thermal management materials and reliability issues in advanced semiconductor packaging.

**CO4:** Apply process integration knowledge to model, simulate, and optimize packaging performance.

**CO5:** Design and present a semiconductor packaging solution integrating materials, processes, and emerging technologies.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	2
CO2	3	3	3	3	3	1	2	1	0	1	0	3	3
CO3	3	3	3	3	3	1	3	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW

2. MODERATE



# **COURSE 6 (Program Elective-01)**

# **Program Elective-01**

PE01A: TFT

PE01B: Display System Design

PE01C: OLED and LCD

## PE01A: TFT

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental principles, structure, and operation of various types of Thin Film Transistors (TFTs).

**CO2:** Describe and compare different thin film deposition techniques (PVD, CVD, ALD) used in TFT fabrication.

**CO3:** Apply fabrication process knowledge to design and analyze TFT structures for electronic and optoelectronic applications.

**CO4:** Evaluate electrical and optical properties of TFTs through appropriate characterization methods.

**CO5:** Design and simulate a TFT-based electronic device considering materials, process, and performance parameters.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						E SPE	RAMM CIFIC OMES
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	3
CO2	3	3	2	2	3	1	2	1	0	1	0	2	3
CO3	3	3	3	3	3	1	2	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	1	1	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW

2. MODERATE



# **PE01B: Display System Design COURSE OUTCOMES:**

**CO1:** Explain the fundamental principles and architectures of various display technologies, including LCD, OLED, and emerging displays.

**CO2:** Analyze user requirements and system specifications to design user-centric display systems.

**CO3:** Evaluate visual quality parameters such as contrast, color accuracy, and viewing angles for optimal display performance.

**CO4:** Integrate emerging technologies such as AR and VR into display system design, addressing design challenges and opportunities.

**CO5:** Design, prototype, and evaluate an innovative display system through systematic design, testing, and user feedback.

# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	3
CO2	3	3	3	2	3	2	1	1	1	2	2	3	3
CO3	3	3	3	3	3	1	2	1	1	1	1	3	3
CO4	3	3	3	3	3	2	3	1	2	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

PE01C: OLEDs and LCDs: Display Technologies

## **COURSE OUTCOMES:**

**CO1:** Explain the fundamental working principles, evolution, and architectures of OLED and LCD technologies.



**CO2:** Analyze material properties, device structures, and fabrication processes involved in OLED and LCD manufacturing.

**CO3:** Evaluate the electrical and optical performance parameters of OLEDs and LCDs, including luminance, color accuracy, contrast, and response time.

**CO4:** Compare and contrast OLED and LCD technologies in terms of performance, fabrication complexity, and application suitability.

**CO5:** Design and present a prototype or case study demonstrating practical understanding of OLED and LCD-based display systems.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	3
CO2	3	3	3	3	3	1	2	1	0	1	0	3	3
CO3	3	3	3	3	3	1	2	1	1	1	1	3	3
CO4	3	3	3	2	3	1	2	1	1	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

# **COURSE 7 (Program Elective-02)**

# **Program Elective-02**

PE02A: FPGA Programming PE02B. Logic Verification PE02C. Design for Testability

**PE02A: FPGA Programming** 

**COURSE OUTCOMES:** 



**CO1:** Explain the architecture, configuration process, and applications of FPGA technology in modern digital systems.

**CO2:** Develop and simulate digital circuits using VHDL and Verilog programming languages.

**CO3:** Design and implement combinational, sequential, and system-level circuits using FPGA hardware platforms.

**CO4:** Integrate IP cores and develop complex FPGA-based systems addressing real-world applications.

**CO5:** Demonstrate project development skills by designing, implementing, and presenting FPGA-based digital solutions.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGI E SPEC OUTCO	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	2
CO2	3	3	3	3	3	1	1	0	1	1	1	3	3
CO3	3	3	3	3	3	1	1	0	2	1	1	3	3
CO4	3	3	3	3	3	1	1	1	2	2	2	3	3
CO5	3	3	3	3	3	2	1	1	3	3	3	3	3

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# **PE02B.** Logic Synthesis

# **Course Outcomes (COs)**

**CO1:** Explain the fundamentals of logic synthesis, Boolean algebra, and HDLs in digital design.

**CO2:** Design and optimize combinational logic circuits using two-level and multi-level synthesis techniques.

**CO3:** Develop and synthesize sequential circuits and FSMs considering timing and performance constraints.

**CO4:** Apply advanced synthesis techniques such as technology mapping, retiming, and logic restructuring for optimization.

**CO5:** Design, implement, and optimize digital circuits through projects using industrial logic synthesis tools.



# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	2
CO2	3	3	3	2	3	1	1	0	1	1	1	3	3
CO3	3	3	3	3	3	1	1	0	1	1	1	3	3
CO4	3	3	3	3	3	1	1	0	1	1	2	3	3
CO5	3	3	3	3	3	2	1	1	3	3	3	3	3

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**PE02C: Design for Testability** 

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental concepts, need, and evolution of design for testability (DFT) in modern VLSI systems.

**CO2:** Implement and analyze Built-In Self-Test (BIST) and scan chain techniques for improving circuit testability.

**CO3:** Develop and simulate fault models using DFT methodologies and tools for detecting potential circuit faults.

**CO4:** Apply various design-for-testability strategies and verify compliance with industrial standards.

**CO5:** Design and present testable VLSI circuits incorporating advanced DFT techniques and current industry practices.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROG E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	2	2	1	1	1	0	1	0	2	2
CO2	3	3	3	3	3	1	1	0	1	1	0	3	3
CO3	3	3	3	3	3	1	1	0	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	2	2	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

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#### **SEMESTER-VI**

# Open Elective-01 (Online)

- A. AI/ML for CAD VLSI
- B. Device Modelling and Simulation
- C. Device and Materials Reliability

# Open Elective-02

- A. Semiconductor Industry Practice & standards
- B. Semiconductor business and marketing
- C. Entrepreneurship in Semiconductors

# Open Elective-02

- A. IC Packaging Techniques
- B. materials for Semiconductor Packaging
- C. Package Design and Simulation Tool

# **COURSE 1 (Open Elective-01 (Online))**

**OE01A: AI/ML for CAD VLSI** 

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamentals of Artificial Intelligence (AI) and Machine Learning (ML) techniques relevant to VLSI CAD applications.

**CO2:** Apply AI/ML techniques for pattern recognition and feature extraction in IC layout design.

**CO3:** Implement ML-based optimization algorithms for improving design automation, layout generation, and rule checking in CAD tools.

**CO4:** Develop ML models for performance prediction of VLSI circuits focusing on power, delay, and reliability.



CO5: Design and evaluate an AI/ML-driven CAD solution through a mini-project or case

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTCO	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	1	1	1	0	1	0	2	2
CO2	3	3	3	3	3	1	1	0	1	1	0	3	3
CO3	3	3	3	3	3	1	1	0	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	1	1	3	3
CO5	3	3	3	3	3	2	2	1	3	3	3	3	3

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# **OE01B: Device Modelling and Simulation**

#### **COURSE OUTCOMES:**

**CO1:** Explain advanced semiconductor physics concepts including carrier statistics, quantum effects, and their influence on modern device behavior.

**CO2:** Develop and analyze models for diodes and BJTs considering non-idealities, high-frequency effects, and temperature dependencies.

**CO3:** Construct and simulate advanced MOSFET and nanoscale transistor models incorporating variability and quantum effects.

**CO4:** Evaluate the performance and trade-offs of emerging transistor technologies such as FinFETs, Nanowire FETs, and Tunnel FETs.

**CO5:** Apply simulation tools and statistical methods to address modeling challenges and validate semiconductor device behavior through projects and case studies.

# **MAPPING OF COS WITH POS AND PSOS**

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTCO	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	3	2	2	2	1	1	1	0	1	0	2	3
CO2	3	3	3	3	3	1	1	0	0	1	0	3	3
CO3	3	3	3	3	3	1	1	0	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	2	2	3	3
CO5	3	3	3	3	3	2	2	1	2	3	3	3	3

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# **OE01C: Device and Materials Reliability**

#### **COURSE OUTCOMES:**

**CO1:** Explain the fundamental concepts and significance of device and materials reliability in semiconductor systems.

**CO2:** Identify and analyze various intrinsic and extrinsic failure mechanisms in semiconductor devices and interconnects.

**CO3:** Evaluate the reliability aspects of materials used in VLSI technologies, including dielectrics, interconnects, and packaging materials.

**CO4:** Apply reliability testing, characterization, and simulation methods to assess device degradation and lifetime.

**CO5:** Examine emerging reliability challenges in advanced, flexible, and AI-driven semiconductor technologies and interpret industrial case studies and standards.

# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROG E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	2	2	2	0	1	0	2	2
CO2	3	3	3	3	2	1	2	1	0	1	0	3	3
CO3	3	3	3	3	3	2	3	1	1	1	1	3	3
CO4	3	3	3	3	3	1	2	1	1	1	2	3	3
CO5	3	3	3	3	3	2	3	2	2	2	2	3	3

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3. SUBSTANTIAL

# **COURSE 2 (Open Elective-02 (Online))**

# OE02A: A. Semiconductor Industry Practice & standards

#### **COURSE OUTCOMES:**

**CO1:** Explain the structure, evolution, and value chain of the global semiconductor industry, including key players and operational segments.



**CO2:** Describe and interpret major industry standards related to semiconductor design, manufacturing, quality, and reliability.

**CO3:** Apply standard design and manufacturing practices—including DFM, IP integration, and EDA workflows—to ensure compatibility and reliability.

**CO4:** Evaluate the role of testing, quality assurance, and supply chain standards in ensuring product reliability and sustainability.

**CO5:** Analyze emerging trends and evolving standards in advanced semiconductor technologies, including AI/ML integration, heterogeneous packaging, and hardware security.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	2	2	2	1	2	2	1	2
CO2	3	3	3	2	3	2	2	2	1	2	2	2	3
CO3	3	3	3	3	3	1	1	1	1	1	2	3	3
CO4	3	3	3	3	3	2	3	2	2	2	2	2	3
CO5	3	3	3	3	3	2	3	2	2	2	2	3	3

1. LOW

2. MODERATE

3. SUBSTANTIAL

#### **OE02B:** Semiconductor business and marketing:

## **COURSE OUTCOMES:**

**CO1:** Describe the structure, stakeholders, and business models of the global semiconductor industry.

**CO2:** Analyze semiconductor market trends, growth drivers, and competitive forces influencing business strategies.

**CO3:** Apply marketing and product lifecycle management principles to develop effective strategies for semiconductor products.

**CO4:** Evaluate pricing models, supply chain logistics, and IP strategies for sustainable semiconductor business operations.

**CO5:** Assess ethical, environmental, and social aspects of semiconductor business practices and propose responsible marketing solutions.



# MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	2	2	2	1	2	2	1	2
CO2	3	3	2	2	3	2	2	2	1	2	3	2	2
CO3	3	3	3	2	3	2	2	2	2	3	3	2	2
CO4	3	3	3	3	3	3	3	2	2	2	3	2	2
CO5	2	2	2	2	2	3	3	3	2	3	3	1	1

1. LOW 2. MODERATE 3. SUBSTANTIAL

**OE02C:** Entrepreneurship in Semiconductors

## **COURSE OUTCOMES:**

**CO1:** Explain the fundamentals of entrepreneurship, innovation processes, and the structure of the global semiconductor ecosystem.

**CO2:** Identify and analyze potential business opportunities, market dynamics, and emerging semiconductor trends.

**CO3:** Develop viable business models, funding strategies, and financial plans for semiconductor start-ups.

**CO4:** Evaluate technology commercialization, IP management, and product scaling strategies for semiconductor ventures.

**CO5:** Demonstrate leadership, ethical practices, and communication skills through preparation and presentation of a semiconductor start-up proposal

# **MAPPING OF COS WITH POS AND PSOS**

OUTCOM	PRO	GRA	ММЕ	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	2	2	1	2	3	2	2	1	2	2	1	2
CO2	3	3	2	2	3	3	2	2	2	2	2	2	2
CO3	3	3	3	2	3	2	2	2	2	3	3	2	2
CO4	3	3	3	3	3	3	3	3	2	2	2	2	2
CO5	2	2	3	2	2	3	3	3	3	3	3	1	1

## 1. LOW 2. MODERATE 3. SUBSTANTIAL

# **COURSE 3 (Open Elective-03 (Online))**

# **OE03A: IC Packaging Techniques**

#### **COURSE OUTCOMES:**

**CO1:** Explain the types, properties, and evolution of semiconductor packaging materials and technologies.

**CO2:** Analyze substrate, die attach, and encapsulation materials with respect to their fabrication and reliability aspects.

**CO3:** Evaluate interconnect materials, bonding techniques, and thermal management methods for enhanced package performance.

**CO4:** Apply design principles to integrate materials, structures, and processes in developing semiconductor packages.

CO5: Propose innovative and sustainable packaging solutions considering emerging technologies and industry practices.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	3	2	2	2	2	2	1	0	1	0	2	2
CO2	3	3	3	3	2	1	2	0	0	0	0	2	3
CO3	3	3	3	3	3	1	2	0	0	1	0	3	3
CO4	3	3	3	3	3	0	2	0	1	1	0	3	3
CO5	3	3	3	3	3	2	3	1	2	3	3	3	3

1. LOW 2. MODERATE 3. SUBSTANTIAL

**OE03C: Package Design and Simulation Tool** 

# **COURSE OUTCOMES:**

**CO1:** Explain the principles, materials, and design considerations of semiconductor packaging.

CO2: Analyze electrical, thermal, and mechanical challenges in package design.

**CO3:** Apply simulation tools to evaluate signal, power, and thermal integrity of packages.

**CO4:** Develop 3D multi-physics models integrating thermal, electrical, and mechanical domains.



CO5: Design, optimize, and document complete semiconductor packages using industry tools.

# MAPPING OF COs WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
CO1	3	3	2	2	2	2	2	1	0	1	0	2	2
CO2	3	3	3	3	2	1	2	0	0	0	0	2	3
CO3	3	3	3	3	3	1	2	0	0	1	0	3	3
CO4	3	3	3	3	3	0	2	0	1	1	0	3	3
CO5	3	3	3	3	3	1	2	1	2	3	3	3	3

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#### **SEMESTER-VIII**

# **COURSE 1 (Final Year Project Phase 2)**

#### **COURSE OUTCOMES:**

C01: Formulate a complex engineering problem by identifying requirements, constraints, and relevant VLSI semiconductor objectives to design or technology. C02: Design a system, component, or process to solve the identified problem, applying devices, VLSI semiconductor principles of design, fabrication. C03: Implement the proposed solution using appropriate hardware description languages, EDA tools, simulation software, experimental or setup. C04: Analyze the results of the implementation through testing, simulation, or measurement, evaluate the solution's performance against specified and criteria. C05: Synthesize the complete project work into a comprehensive report and presentation, demonstrating professional communication and ethical responsibility.

#### MAPPING OF COS WITH POS AND PSOS

OUTCOM	PRO	GRA	MME	OUT	COM	ES						PROGE E SPEC OUTC	
ES	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO1 0	PO1 1	PSO1	PSO2
C01	3	3	2	3	-	1	1	1	1	2	3	3	3
C02	3	3	3	2	2	2	1	2	2	2	2	3	3
C03	3	2	3	2	3	-	2	2	2	2	2	3	3
C04	3	3	3	3	3	2	2	2	2	2	2	3	3
C05	2	2	2	2	-	2	3	3	3	3	3	2	2

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